



# Sierra Components, Inc.

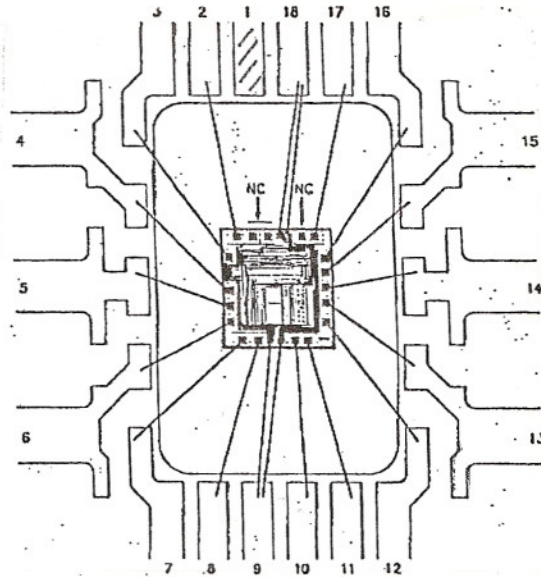
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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

NOTE: I.D.T. LOGO, LOWER LEFT

Q1	24643	7049: 24643 No 3115
Q0	22961	7049: 24643 No 3115
REV	DCN	DATE APPROVAL
BILL OF MATERIAL		
DESCRIPTION		
DIE 72402 REV. Y		
SIZE 2050 μm X 2320 μm		
WIRE Al MA .00125 IN.		
NO. OF WIRES 19		
STOCK NO.	PACKAGE / LEADFRAME / I/O / ETC.	
30-013-018	CD18 FRAME MSC-0814	
20-049-018	CD18 NO-AU(-187)BASE MSC-0228	
21-049-018	CD18 (-187) CAP MSC-0225	
41-003-003	D/A Ag GLASS MSC-0514	
ASSEMBLY DRAWING		
Integrated Device Technology, Inc.		



**Topside Metal: Al**  
**Backside: Si**  
**Backside Potential:**  
**Mask Ref:**  
**Bond Pads : .004"**

APPROVED BY: CB

MFG: IDT

DIE SIZE : .075" x .082"

THICKNESS: .020"

DATE: 2/7/01

P/N: IDT72402L